Amendments to the Specification:

Please change the title of the application on page 1 to the following amended title:

DIGITAL STILL CAMERA WITH MULTIPLE PROCESSORS ~~SYSTEM AND METHOD~~

Please replace the cross reference paragraph on page 1 with the following amended paragraph:

This application claims priority from provisional applications Serial Nos. 60/172,780, filed 12/20/99; 60/176,272, filed 1/14/00; 60/177,432, filed 1/21/00; 60/214,951, filed 06/29/00; and 60/215,000, filed 06/29/00. The following pending US patent applications disclose related subject matter and have a common assignee with the present application: ~~Serial No. , filed ...~~ Appl. Nos.: 09/743,992; 09/743,258; 09/745,136; 09/745,134; 09/742,944; 09/745,132; 09/745,135; 09/745,133, all filed 12/20/2000.

Please replace the brief description of drawings on pages 2-3 with the following amended brief description.

Figures 1a-1b show a preferred embodiment system in functional block format.

Figures 2-6 illustrate data flows.

Figures 7a-7b show CFA arrangements.

Figure 8 is a functional diagram for white balance.

Figures 9a-9c ~~9a-9b~~ show RGB gain and gamma correction.

Figures 10a-10l ~~Figure 10~~ illustrates CFA interpolation.

Figure 11 ~~Figures 11a-11b~~ shows color conversion.

Figures 12a-12b show a memory controller data flow.

Figures 13a-13b illustrate burst mode compression/decompression data flow and symmetrical Huffman table use.~~Figure 13 is a functional block diagram of a burst compression/ decompression engine.~~

Figure 14 is a functional block diagram of a preview engine.

Figure 15 is an on screen display block diagram.

Figure 16 is an on screen display window.

Figure 17 shows a hardware cursor.

Figures 18a-18b ~~Figure 18~~ illustrates a DSP subsystem.

Figure 19 shows parallel multiply-accumulate datapath.

Figure 20 shows a coprocessor architecture.

Figure 21 illustrates a look-up table accelerator.

Figure 22 is a block diagram of a variable length coder.

Figures 23a-23b ~~Figure 23~~ shows a bridge.

Figure 24 shows multiprocessor debugging support.

Figure 25 illustrates UART connections.

Figure 26 is a block diagram of flash card/smart card interface.

Figures 27-38 illustrate color filter array interpolations.

Figures 39a-39b and 40 show white balancing.

Figures 41a-41b ~~41a-4ab~~ and 42a- 42e indicate image resizing.

Figures 43-45 illustrate tone-scaling.

Figures 46a-46b and 47-48 show synchronization.

Figures 49-52 ~~49-52~~ show decoding buffering.

Please replace the first paragraph on page 14 with the following amended paragraph:

After the CFA interpolation and color correction, the pixels are typically in the RGB color space. Since the compression algorithm (JPEG) is based on the YCbCr color space, a color space transformation must be carried out. Also the preferred embodiment DSC generates a NTSC signal output for display on the TV and also to feed into the LCD preview. Hence an RGB to YCbCr color space conversion needs to be carried out. This is a linear transformation and each Y, Cb, Cr value is a weighted sum of the R, G, B values at that pixel location. Figure ~~11a~~ 11 illustrates the color conversion as realized in the hardwired preview engine. The DSP (playback) implementation is similar in principle but allows a higher precision conversion:

Please replace the last paragraph on page 14 with the following amended paragraph:

The edge enhancement is a high pass filter; this high pass filter also amplifies the noise. To avoid this amplified noise, a threshold mechanism is used to only enhance those portion of the image lying on an edge. The amplitude of the amplified edge may vary. The threshold operation is necessary to reduce amplification of noise. Therefore, only those pixels get enhanced which are an element of an edge. ~~The enhancement signal added to the luminance channel can be represented graphically as in Figure 11b; the parameters t1, t2, and the slope s1 can be chosen as seen necessary to obtain the best quality.~~

Please replace the middle paragraph on page 51 with the following amended paragraph:

The preferred embodiment DSC engine includes an improved Burst Capture function with real-time processing, without compromise in the image resolution as compared to the regular capture mode. The Burst Capture Mode is the use of dedicated compression and decompression engine 108 for an increased burst capture sequence length. A sequence of CCD raw image frames is first stored in SDRAM 160 by using Compression engine 108; see Figure 13a. Then, as an off-line process, the image pipeline of regular capture mode retrieves the CCD raw images from SDRAM 160, processes them sequentially, and finally stores them back as JPEG files in the SDRAM. The Animated Playback Mode can display these JPEG files.

Please replace the last paragraph on page 51 with the following amended paragraph:

Burst mode compression/decompression engine 108 includes differential pulse code modulation (DPCM) and Huffman coding using the same tables as the entropy-coding of DC coefficients in baseline JPEG compression. Engine 108 uses the sample Huffman table in the JPEG standard for chrominance DC differential data. Engine 108 also provides the inverse transforms as illustrated in Figure ~~13~~13b. Fixed Huffman Table (JPEG Huffman table for Chrominance DC coefficients):